**Tips：**

1. Because PCB manufacture’s process limit, we have to meet their requirements. Mainly Via to line, Drill hole to line MIN spacing.
2. To know whether this PCB can meet more strict spacing constrain, we tried to modify it. After several days trying, we found that it was realizable, and we re-layout some areas(have big changes) using our style. It is only for your reference.
3. Top layer basically has not changed. Main changes are in internal layers and bottom layers.
4. Connector Hole can’t remove pin’s suppression in internal layers. Such as J6. It has risk when connector in plug in/out. We fixed it.
5. It is better to add route-keepout near board’s outlines. It will cut off coppers on the edge of board. Otherwise, it has risk to be short by residuary copper after board’s outline cut off. We added this route-keepout on PCB.
6. This PCB’s thickness will be 0.20mm-0.22mm.

**Main constrains changes**

1. We set space/physical constrains in BGA area:

**Via to line:** (all set to conductor layer)

Top/Bottom layers: >=0.14mm

Internal Layers: >=0.18mm

**Hole to line:**

Top/Bottom layers: >=0.20mm

Internal Layers: >=0.20mm

1. We set space/physical constrains in default area:

**Via to line:** (all set to conductor layer)

Top/Bottom layser: >=0.15mm

Internal Layers: >=0.18mm

**Hole to line:**

Top/Bottom layers: >=0.254mm

Internal Layers: >=0.254mm

Above two points are the main requirements from PCB manufacture. Below almost all modified actions are according to them.

1. We reduce some lines(include differential pairs, and DDR’s data/address single lines) width and Min line spacing:

Top/Bottom layers(line width): 0.10mm, differential primary Gap: 0.10mm, single line to line spacing: 0.10mm

Internal layers(line width): 0.075mm, differential primary Gap: 0.13mm(\*Note2), single line to line spacing: 0.075mm

1. For Via, basically no changed(0.20mm/0.45mm).
2. Others setting, Via to Via, Via to shape, shape to shape, and so on, please check PCB’s constrains.

**PCB layout main changes**

1. Fix Error because modify space constrain
   1. Most errors can be easily fixed.
   2. Some errors in DDR/FPGA fanout areas are not easy to fix, need to re-layout some lines, and change some FPGA pins fanout.
2. Differential pairs setting(Internal Layers/Bottom Layers)
   1. We found that differential pair can use same setting in whole layer(whether internal layer or bottom layer, whether BGA area or default area). If so, their differential impendence will keep as same value. And PCB manufacture can use same materials in internal layers which need control differential pairs impendence to 100ohm. So we set differential pair’s Min line spacing equal to primary gap(0.13mm), line width is 0.075mm(=Min width, = Neck width). We re-layout all differential pairs in internal layers.
   2. Bottom layer, ADC\_OUT\_A/B/C/D, use setting(line width =0.10mm, primary gap =0.10mm). We re-layout these 4 differential pairs in bottom layer.
3. PS/PL DDR4 areas
   1. DDR’s data/address single impendence should be 50 ohm, so their line width =0.075mm in internal layers, and =0.10mm in bottom layer。
   2. We found that we need add some GND via in PS/PL areas. And to keep DDR’s data/address in GND via, we re-layout these nets.
   3. We follow DDR’s constrains, and set more restrict match group tolerance as below.
      1. DQS +/-(2)：0.0254mm(1mil)
      2. Data one bytes(11)：0.0254mm(1mil)
      3. Data All byte(2 or 4): 2.54mm(100mil)
      4. CLK +/-(2)：0.0254mm(1mil)
      5. Address(from FPGA’s PIN to DDR’s PIN)(29)：0.254mm(10mil).
      6. PS DDR4 has 2 chips, so there are CLK\_U4\_U46(2), CLK\_U4\_U14(2), CLK\_U14\_R(2)(terminal resistors), Address\_U4\_U46(2), Address\_U4\_U14(2), Address\_U14\_R(29)(terminal resistors).
      7. PL DDR4 has 1 chip, so there are CLK\_U4\_U12(2), CLK\_U12\_R(2)(terminal resistors), Address\_U4\_U12(27), Address\_U12\_R(27)(terminal resistors).
   4. We adjust delay tune type, use smaller height tune. Some paper said that smaller height tune will cause smaller cross-talk noise.
4. We add all differential pairs to match group, to check their layout length tolerance. Such as VINA/B/C/D, some clock+/-, FPGA DIFF Lines to J5.
5. BGA’s top layer, we placed a GND void on it, it will be help in assembly stage.
6. Silkscreen maybe need to re-adjust, we didn’t check it.